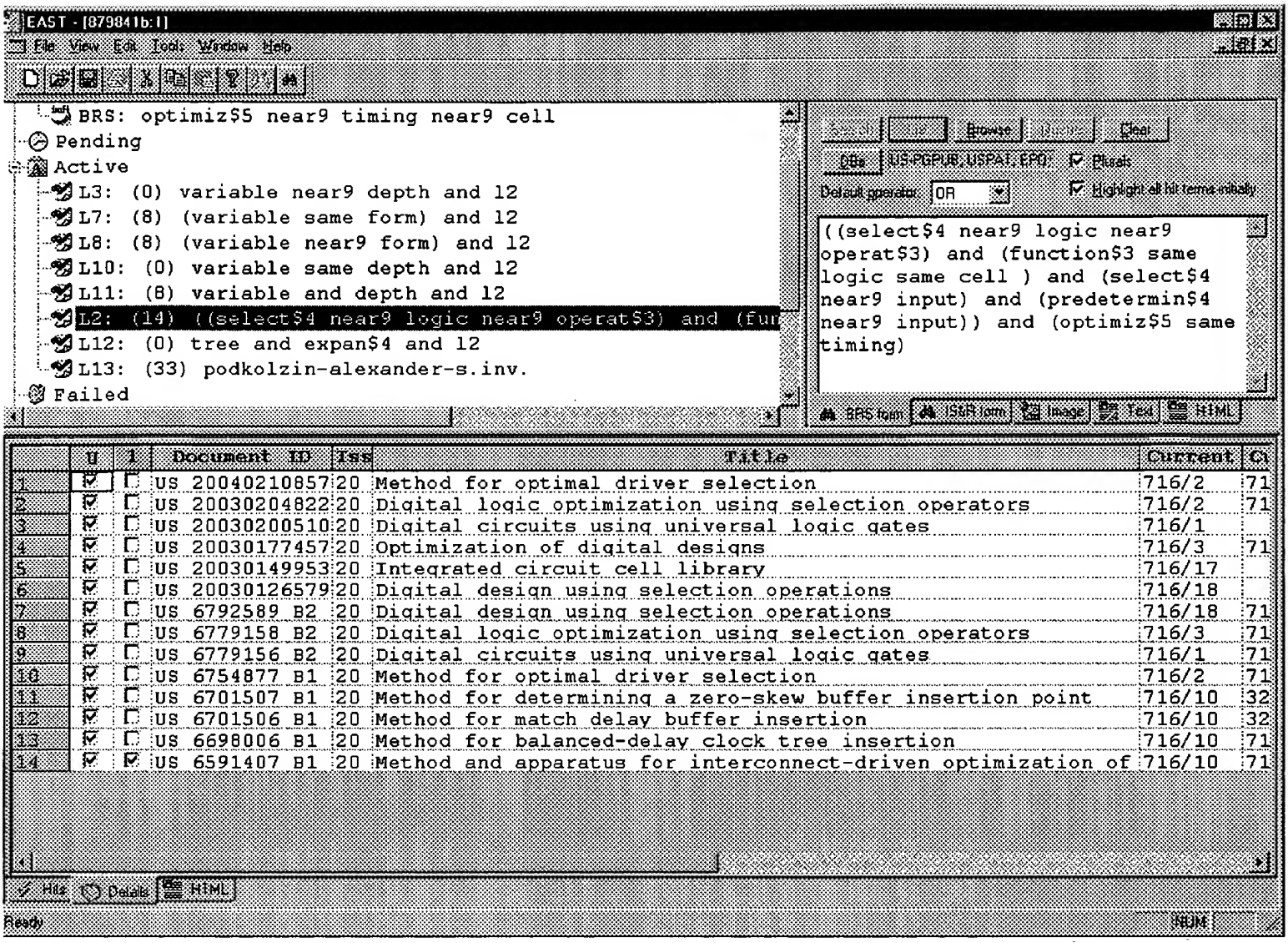
EAST - [879841b:1]
File View Edit Tools Window Help
BRS: optimiz$5 near9 timing near9 cell
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L3: (0) variable near9 depth and l2
L7: (8) (variable same form) and l2
L8: (8) (variable near9 form) and l2
L10: (0) variable same depth and l2
L11: (8) variable and depth and l2
L2: (14) ((select$4 near9 logic near9 operat$3) and (fur
L12: (0) tree and expan$4 and l2
L13: (33) podkolzin-alexander-s.inv.
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OR
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((select$4 near9 logic near9 operat$3) and (function$3 same logic same cell) and (select$4 near9 input) and (predetermin$4 near9 input)) and (optimiz$5 same timing)
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1 US 20040210857 20 Method for optimal driver selection 716/2 71
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3 US 20030200510 20 Digital circuits using universal logic gates 716/1
4 US 20030177457 20 Optimization of digital designs 716/3 71
5 US 20030149953 20 Integrated circuit cell library 716/17
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9 US 6779156 B2 20 Digital circuits using universal logic gates 716/1 71
10 US 6754877 B1 20 Method for optimal driver selection 716/2 71
11 US 6701507 B1 20 Method for determining a zero-skew buffer insertion point 716/10 32
12 US 6701506 B1 20 Method for match delay buffer insertion 716/10 32
13 US 6698006 B1 20 Method for balanced-delay clock tree insertion 716/10 71
14 US 6591407 B1 20 Method and apparatus for interconnect-driven optimization of 716/10 71
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Details
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